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Question Paper Code : 20457

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2022.

Sixth/Seventh Semester

Electrical and Electronics Engineering

EC 8095 — VLSI DESIGN

(Common to : Electronics and Communication Engineering / Electronics and Instrumentation Engineering / Electronics and Telecommunication Engineering / Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Sketch a complementary CMOS gate computing W=(XY+YZ)'
2. Write the expression for parasitic delay & logical effort of an N-input NAND gate.
3. What is the use of transmission gates?
4. List the sources of power dissipation in CMOS circuits.
5. What is meant by bistability?
6. Define clock-skew and clock-jitter.
7. Draw the circuit diagram of 1-bit binary shifter using MOS transistor.
8. State the need of sense amplifier in a memory cell.
9. What is the significance of field programmable gate arrays?
10. What are limitations of IDDQ testing?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the DC transfer characteristics of CMOS inverter. (6)

(ii) Estimate the delay of CMOS logic gates as the RC product of the effective driver resistance and the load capacitance. (7)

Or

(b) Write the layout design rules and draw the diagram for 4 input NAND and NOR gates.

12. (a) Explain pass transistor logic and show how complementary pass transistor logic and double pass transistor logic applied for 2:1 MUX.

Or

(b) Sketch a combinational function $Y = (AB + CD)'$.

(i) Pseudo-nMOS logic (4)

(ii) Domino logic (4)

(iii) Cascode voltage switch logic. (5)

13. (a) Explain the circuit and working of CMOS implementation of Schmitt trigger.

Or

(b) (i) Describe the concept of pipelining in sequential circuits with suitable example. (7)

(ii) Sketch and explain monostable sequential circuits based on CMOS logic. (6)

14. (a) (i) Explain the concept of carry look-ahead adder with neat diagram. (9)

(ii) Discuss trade-off between speed Vs area. (4)

Or

(b) Elucidate in detail the design of low power SRAM memory circuits.

15. (a) Describe FPGA interconnect routing resources with neat diagram.

Or

(b) Explain three main approaches commonly used for Design for Testability (DFT).

PART C — (1 × 15 = 15 marks)

16. (a) Realize a 2-input EXOR using static CMOS, transmission gate and dynamic CMOS logic. Analyze the hardware complexity.

Or

(b) Apply radix-2 encoding to realize a 4 big signed multiplier for $(-11)\times(-12)$. For the same multiplier apply radix-8 booth encoding and justify the advantages between radix-4 and radix-8 booth multiplier.